

Bipolar Transistor Amplifiers

Purpose

The aim of this experiment is to construct a bipolar transistor amplifier with a voltage gain of minus 25. The amplifier must accept input signals from a source with an impedance of $1\text{ k}\Omega$ and provide an undistorted output amplitude of 5 V when driving a $560\ \Omega$ load. The bandwidth should extend from below 100 Hz to above 1 MHz .

Introduction

An electrical signal can be amplified using a device which allows a small current or voltage to control the flow of a much larger current from a dc power source. Transistors are the basic device providing control of this kind. There are two general types of transistors, bipolar and field-effect. The difference between these two types is that for bipolar devices an input current controls the large current flow through the device, while for field-effect transistors an input voltage provides the current control. In this experiment we will build a two-stage amplifier using two bipolar transistors.

In many practical applications it is better to use an op-amp as a source of gain rather than to build an amplifier from discrete transistors. A good understanding of transistor fundamentals is nevertheless essential because op-amps are built from transistors. We will learn about digital circuits in Experiment #9, which are also made from transistors. In addition to the importance of transistors as components of op-amps, digital circuits, and an enormous variety of other integrated circuits, single transistors (usually called “discrete” transistors) are used in many circuit applications. They are important as interface devices between integrated circuits and sensors, indicators, and other devices used to communicate with the outside world. High-performance amplifiers operating from DC through microwave frequencies use discrete transistor “front-ends” to achieve the lowest possible noise. Discrete transistors are generally much faster than op-amps. The device we will use this week has a gain-bandwidth product of 300 MHz .

The three terminals of a bipolar transistor are called the emitter, base, and collector (Figure 7.1). A small current into the base controls a large current flow from the collector to the emitter. The current at the base is typically about 1% of the collector-emitter current. This means that the transistor acts as a current amplifier with a typical current gain of ~ 100 . Moreover, the large collector current flow is almost independent of the voltage across the transistor from collector to emitter. This makes it possible to obtain a large amplification of voltage by having the collector current flow through a resistor. We will begin by constructing a common emitter amplifier, which operates on this principle.

A major fault of a single-stage common emitter amplifier is its high output impedance. This can be addressed by adding an emitter follower as a second stage. In this circuit the control signal is again applied at the base, but the output is taken from the emitter. The emitter voltage precisely follows the base voltage but more current is available from the emitter. The common emitter stage and the emitter follower stage are the most common bipolar transistor circuit configurations.

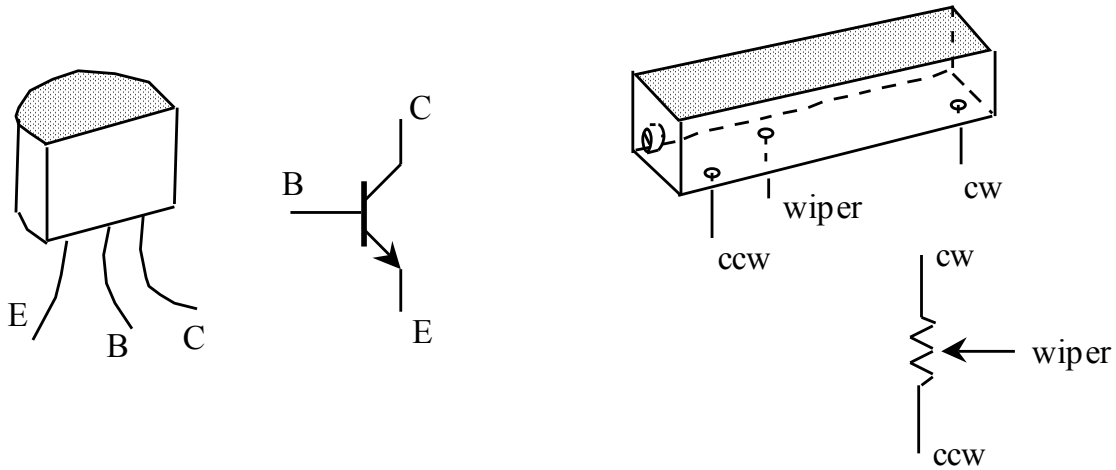


Figure 7.1 Pin-out of 2N3904 and 1 k trimpot

Optional Readings

1. FC chapters 5 (bipolar junction transistors) & 6 (common emitter amplifier)
2. A data sheet for the 2N3904 transistor is posted on our course web site.
3. Horowitz and Hill, Chapter 2. The most important sections are 2.01–2.03, 2.05, the first page of 2.06, 2.07, 2.09–2.12, and the part of 2.13 on page 84 and 85. Have a look at Table 2.1 and Figure 2.78 for a summary of the specifications of some real devices.
4. Bugg gives a brief account of the solid state physics behind transistor operation in Chapter 9. In Chapters 17 and 18 he discusses transistor circuit design in the language of h-parameters and hybrid equivalent circuits, *i.e.* with more mathematical detail than is normally required for circuit design.

Theory

CURRENT AMPLIFIER MODEL OF BIPOLAR TRANSISTOR

From the simplest point of view a bipolar transistor is a current amplifier. The current flowing from collector to emitter is equal to the base current multiplied by a factor. An npn transistor like the 2N3904 operates with the collector voltage at least a few tenths of a volt above the emitter voltage (typically $\sim 0.6\text{V}$ above the emitter voltage), and with a current flowing *into* the base. (There are also pnp transistors with opposite polarity voltages and currents.) The base-emitter junction then acts like a forward-biased diode with a 0.6 V drop: $V_B \approx V_E + 0.6\text{V}$. Under these conditions, the collector current is proportional to the base current: $I_C = h_{FE} I_B$. The constant of proportionality ('current gain') is called h_{FE} because it is one of the "h-parameters," a set of numbers that give a complete description of the small-signal properties of a transistor (see Bugg Section 17.4). It is important to keep in mind that h_{FE} is not really a constant. It depends on collector current (see H&H Fig. 2.78), and it varies by 50% or more from device to device. If you want to know the emitter current rather than the collector current you can find it by current conservation: $I_E = I_B + I_C = (1/h_{FE} + 1) I_C$. The difference between I_C and I_E is almost never important since h_{FE} is normally in the range 100 – 1000. Another way to say this is that the base current is very small compared to the collector and emitter currents.

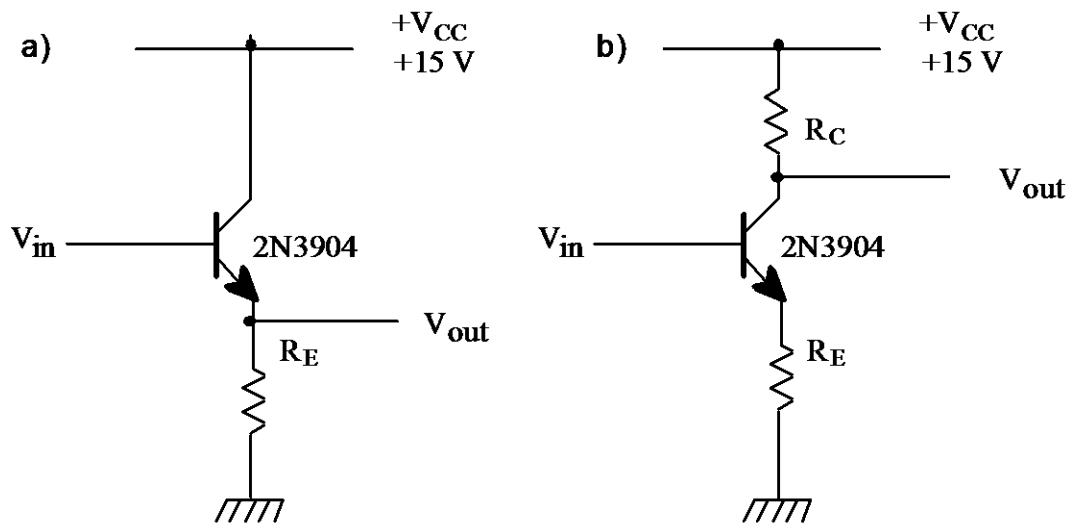


Figure 7.2 a) Emitter follower stage b) Common Emitter Stage

Figure 7.2 shows the two main bipolar transistor circuits we will consider. In the emitter-follower stage the output (emitter) voltage is always 0.6V (one diode drop) below the input (base) voltage. A small signal of amplitude δV at the input will therefore give a signal δV at the output, i.e. the output just “follows” the input. As we will see later, the advantage of this circuit that it has high

input impedance and low output impedance. In the common emitter stage of figure 7.2b, a small signal of amplitude δV at the input will again give a signal δV at the emitter. This will cause a varying current of amplitude $\delta V / R_E$ to flow from the emitter to ground, and hence also through R_C . This current generates a V_{out} of $-R_C(\delta V / R_E)$. Thus the common emitter stage has a small-signal voltage gain of $-R_C/R_E$.

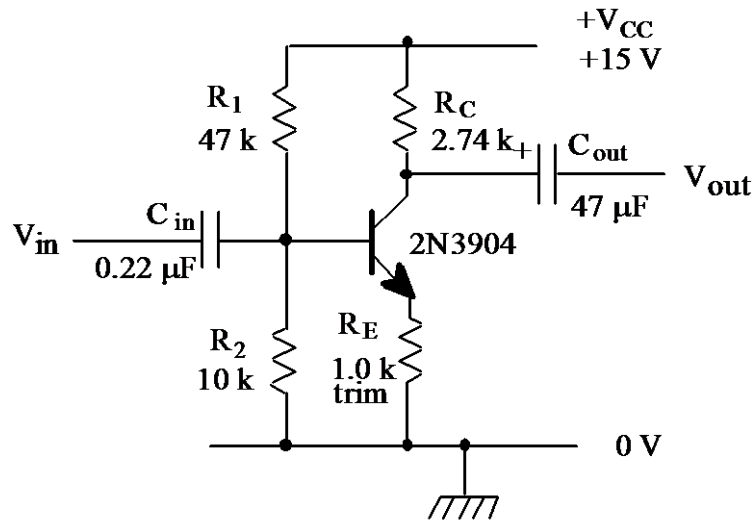


Figure 7.3 Biased Common Emitter Amplifier

Although we usually want to amplify a small ac signal, it is nonetheless very important to set up the proper “quiescent point”, the dc voltages present when the signal is zero. The first step is to fix the dc voltage of the base with a voltage divider (R_1 and R_2 in Figure 7.3). The emitter voltage will then be 0.6 V less than the base voltage. With the emitter voltage known, the current flowing from the emitter is determined by the emitter resistor: $I_E = V_E/R_E$. For an emitter follower, the collector is usually tied to the positive supply voltage V_{CC} . The only difference between biasing the emitter follower and biasing the common emitter circuit is that the common emitter circuit always has a collector resistor. The collector resistor does not change the base or emitter voltage, but the drop across the collector resistor does determine the collector voltage: $V_C = V_{CC} - I_C R_C$.

There are three subtleties to keep in mind when biasing common-emitter or emitter-follower circuits. First of all, the base bias voltage must be fixed by a low enough impedance (parallel combination of R_1 and R_2) so that changes in the base quiescent current do not substantially alter the base voltage. This is essential because the base current depends on h_{FE} and so it is not a well determined quantity. If the base voltage is determined by a divider (as in Figure 7.3), the divider impedance will be low enough when:

$$R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} \ll h_{FE} R_E \quad (1)$$

As we will see in a moment, this equation just says that the impedance seen looking into the divider

(the Thevenin equivalent or $R_1 \parallel R_2$) should be much less than the impedance looking into the base. Another point to keep in mind is that when you fix the quiescent point by choosing the base divider ratio and the resistors R_E and R_C , you are also fixing the dc power dissipation in the transistor which is the product of the voltage across the transistor and the current through it: $P = (V_C - V_E) I_E$. Be careful that you do not exceed the maximum allowed power dissipation P_{\max} . Finally, the quiescent point determines the voltages at which the output will clip or distort. For a common emitter stage, the maximum output voltage will be close to the positive supply voltage V_{CC} . The minimum output voltage occurs when the transistor saturates, which happens when the collector voltage is no longer at least a few tenths of a volt above the emitter voltage. We usually try to design common emitter stages for symmetrical clipping, which means that the output can swing equal amounts above and below the quiescent point.

The voltage gain of the emitter follower stage is very close to unity. The common emitter stage, in contrast, can have a large voltage gain:

$$A = -\frac{R_C}{R_E} \quad (2)$$

If we are interested in the ac gain, then we can replace R_C and R_E with the ac impedances attached to the collector and emitter, which may be different from the dc resistances. In our circuit we use C_E to bypass part of the emitter resistor at the signal frequency (see Fig. 7.4 below).

INPUT AND OUTPUT IMPEDANCES

The input impedance is the same for both emitter followers and common emitter stages. The input impedance looking into the base is

$$r_{in} = (h_{FE} + 1)R \quad (3)$$

In this expression R is whatever impedance is connected to the emitter. For a common emitter stage, R would usually just be the emitter resistor, but for an emitter follower R might be the emitter resistor in parallel with the input impedance of the next stage. If you want the input impedance of the whole stage, rather than just that looking into the base, you will have to consider r_{in} in parallel with the base bias resistors.

The output impedance of a common emitter stage is just equal to the collector resistor R_C .

The output impedance looking into the emitter of an emitter follower is given by

$$\boxed{r_{out} = \frac{R}{h_{FE} + 1}} \quad (4)$$

Now R stands for whatever impedance is connected to the base. Usually this impedance is in parallel with whatever impedance is connected to the emitter.

EBERS-MOLL MODEL OF BIPOLAR TRANSISTOR

A slightly more detailed picture of the bipolar transistor is required to understand what happens when the emitter resistor is very small. Instead of using the current amplifier model, one can take the view that the collector current I_C is controlled by the base-emitter voltage V_{BE} . The dependence of I_C on V_{BE} is definitely not linear, rather it is a very rapid exponential function. The formula relating I_C and V_{BE} is called the Ebers-Moll equation (It is discussed in H&H Section 2.10.)

For our purposes, the Ebers-Moll model only modifies our current amplifier model of the transistor in one important way. For small variations about the quiescent point, the transistor now acts as if it has a small internal resistor r_e in series with the emitter

$$\boxed{r_e = 25 \Omega \left(\frac{1 \text{ mA}}{I_C} \right)} \quad (5)$$

The magnitude of the intrinsic emitter resistance r_e depends on the collector current I_C .

The presence of the intrinsic emitter resistance r_e modifies the above Equations (1) – (4). In Equations (1) and (2) we should substitute $R_E \rightarrow R_E + r_e$, and for Equation (3) we need to substitute $R \rightarrow R + r_e$. Equation (4) is modified to read

$$r_{out} = \frac{R}{h_{FE} + 1} + r_e \quad (4')$$

The most important of these results is the modified Equation (2)

$$\boxed{A = -\frac{R_C}{R_E + r_e}} \quad (2')$$

which shows that the common emitter gain does not go to infinity when the external emitter resistor goes to zero. Instead the gain goes to the finite value $A = -R_C / r_e$.

Pre-Lab Problems

1. (3 points) Calculate the quiescent voltages (the DC voltages with no signal present) V_B , V_E , and V_C , and the currents I_E and I_C for the common emitter circuit in Figure 7.3. You may assume that h_{FE} is so large that the base current is negligible. How much power is dissipated in the transistor itself? Is the power safely below P_{max} ? See 2N3904 data sheet posted on our web site. What is the maximum h_{FE} value at 10 mA collector current? (You may use this value for calculations below.)
2. (2 points) Find the ac voltage gain of the circuit in Figure 7.4 (see below) for 15 kHz sine waves with the emitter bypass capacitor C_E removed.
3. (2 points) The emitter bypass capacitor can provide an ac ground path for the emitter, increasing the gain of the amplifier at high frequency. Considering the effects of the intrinsic emitter resistance r_e , what is the maximum possible ac voltage gain of the amplifier in Figure 7.4 (assume $I_C \approx 2$ mA)?
4. (3 points) What setting of the emitter trimpot is needed to give the required gain of -25 ? (Do not assume $r_e = 0$.) For the single stage in Figure 7.4, what are the input and output impedances r_{in} and r_{out} at 15 kHz and a gain of -25 ? Note that r_{in} is the impedance looking into the base in parallel with the base divider impedance. Calculate the fraction of the original amplitude obtained when a 560Ω load is connected to the output via a coupling capacitor (C_{out} in Fig. 7.4).

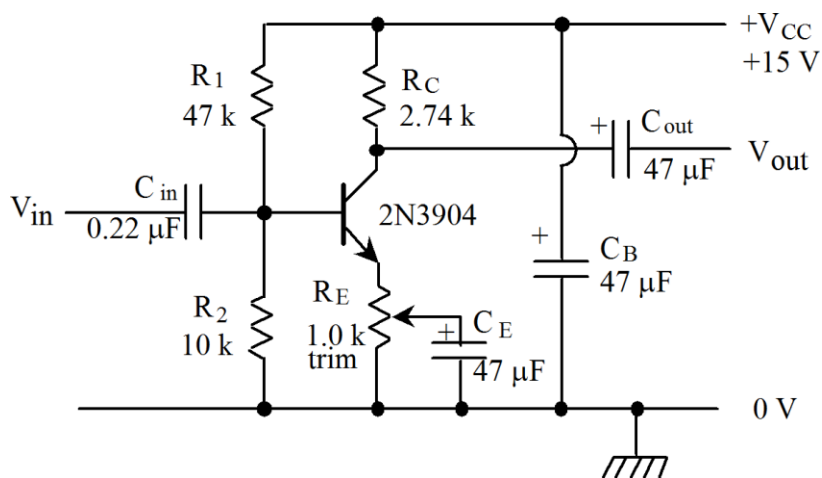


Figure 7.4 Common Emitter Stage Layout and Schematic

New Apparatus and Methods

A drawing to help you identify the leads of the 2N3904 transistor and the trimpot is shown in Figure 7.1. The 2N3904 is an npn device, as indicated by its symbol with an outward pointing

arrow. The arrow for a pnp device points in. To keep the convention straight, remember Not Pointing in for npn. Your trimpot may not look exactly like the one shown, but it will have the three leads wiper, cw, and ccw. The wiper moves toward the cw lead when the screw is turned clockwise. The transistor amplifier uses dc power at +15 V only.

Figure 7.4 shows the first amplifier stage. When you build it, make sure to keep all wires that connect to the transistor at a minimum length. Otherwise, you risk spontaneous oscillations in your circuit due to the very large gain of the transistor. The base and emitter must not be on adjacent strips or the circuit will oscillate. Your circuit will be easier to understand if you try to keep the physical layout looking like the schematic diagram.

Use the oscilloscope 10x probe to observe the amplifier outputs. The 10x probe minimizes capacitive loading and reduces the risk of spontaneous oscillations.

Experiment

POLARITY CHECK

Determine the polarities of the emitter-base and base-collector diode junctions of a 2N3904 and 2N3906 using the diode tester on your digital multimeter. This function is enabled by turning the selector on the DMM to the diode symbol. The meter will beep when current is flowing. Touch the meter leads together to hear the beep. Attach the leads to a 1N4002 or a 1N4148 diode which are simple pn junctions. The DMM will beep when the red lead is attached to the anode “p” and the black lead is connected to the cathode “n” (indicated by a stripe). It will not beep if the connections are reversed. Also, the meter will read the voltage drop (typically 0.6 V) across the pn junction when the polarity is correct.

(1) Is the 2N3904 an npn or a pnp transistor? Is the 2N3906 and npn or pnp? The pin-out (pin configuration) for a 2N3906 is the same as for a 2N3904.

COMMON EMITTER AMPLIFIER: QUIESCENT STATE

The first step is to construct the bias network and check that the correct dc levels (quiescent voltages) are established. Assemble the common emitter stage as shown in Figure 7.4, but without the input and output coupling capacitors or the emitter capacitor (without C_{in} , C_{out} , and C_E). The wiper contact on the emitter resistor R_E should not be connected to anything yet. Measure the resistors before putting them in the circuit, and if they differ from the values used in your calculations, recalculate the quiescent voltages. (You could also combine two or three resistors to match your initial values better, but this would increase the complexity and make it a harder to change the circuit later.) Before turning on the power, disconnect the power supply from the circuit

board for a moment and check that it is set to +15 V. Then turn on the power, and check the dc levels V_B (at the transistor base), V_E (at the emitter) and V_C (at the collector).

The quiescent levels should agree with your calculations to within about 10%. If they do not, there is something wrong that should be corrected before you go on.

COMMON EMITTER AMPLIFIER: FIXED GAIN

Convert the previous circuit to an AC amplifier by adding the coupling capacitors C_{in} and C_{out} . Be sure to observe the polarity of polarized capacitors! The capacitors will transmit ac signals but block dc signals. This allows you to connect signals without disturbing the quiescent conditions.

When you switch on the power, you may see high frequency spontaneous oscillations. These must be suppressed before you can proceed. A bypass capacitor ($\sim 100\text{nF}$) between +15V and ground close to the transistor may help.

Assemble a test set-up to observe the input and output of the amplifier with 15 kHz sine waves, using the 10x scope probe for the output. You may need to add a 220 k Ω resistor to ground after C_{out} to keep the dc level at the scope input near ground. Vary the input amplitude to find the output amplitude at which clipping begins.

Measure the gain of the amplifier for 15 kHz sine waves at an amplitude about half the clipping level. While you are at the bench, compare the measured gain with that predicted from the measured values of components:

$$A = -\frac{R_c}{R_E + r_e}$$

Comment on the comparison. If the values differ by more than 20% find the cause and correct the problem before you go ahead.

COMMON EMITTER AMPLIFIER-VARIABLE GAIN

Connect the wiper of the 1.0 k Ω trim-pot R_E through the bypass capacitor C_E to ground. Verify that the quiescent point has not changed significantly. Observe the change in gain as you traverse the full range of the trimpot using 15 kHz sine waves. Start with the wiper at ground (bottom of diagram) and move it up until C_E bypasses all of R_E . Always measure V_{in} and V_{out} when measuring the gain of a circuit. Do not rely on the number displayed on your function generator for V_{in} .

When approaching maximum gain turn down the input amplitude (a long way) so that the output signals are still nicely shaped sine waves. (If you can't make it small enough, put a 5 Ω resistor to ground at the output of the function generator. This will reduce the amplitude of the signal at the

input of your circuit by a factor of 10.) If the output is distorted the amplifier is not behaving linearly, and our formulas for the ac gain are not correct.

Compare the measured maximum gain with the value predicted in the homework for several input voltages (and hence output amplitudes V_{out}) going down by factors of two. Do theory and experiment converge as V_{out} approaches zero?

COMMON EMITTER AMPLIFIER: INPUT AND OUTPUT IMPEDANCE

Set the amplifier gain to -25 for 15 kHz sine waves. What trimpot setting gives a gain of -25 ? (To see where the trimpot is set, remove it from the circuit and measure the resistance from cw to wiper or from ccw to wiper.)

Simulate the required source impedance by inserting a 1 k Ω resistor in series with the input. In other words, the signal from the generator passes through a 1 k Ω resistor before going to the amplifier input. What fraction of the original output amplitude do you see? Is this as expected? Remove the 1 k Ω resistor before the next test so that you test only one thing at a time.

Connect a 560 Ω load from the output to ground. What fraction of the original output do you now see? Is this as expected (why/why not)?

EMITTER FOLLOWER OUTPUT STAGE

In the emitter follower circuit, the input signal is applied to the base of the transistor, but the output is taken from the emitter. The emitter follower has unit gain, *i.e.* the emitter "follows" the base voltage. The input impedance is high and the output impedance is low.

Ordinarily the quiescent base voltage is determined by a bias circuit. In the present case, the collector voltage V_C of the previous circuit already has a value suitable for biasing the follower, so a direct dc connection can be made between the two circuits.

Assemble the emitter follower circuit shown in Figure 7.5. Do NOT connect the 560 Ω load to the output yet.

Carry out appropriate dc diagnostic tests without the function generator connected to the input. This time we expect the collector to be at +15 V, the base to be at the collector voltage of the first stage, and the emitter to be about 0.6 V below the base. Correct any problems before moving on.

Confirm that the voltage gain of the emitter follower is unity. Drive the complete system with the function generator. Observe the ac amplitudes at the input of the emitter follower and at the output. Measure the ac gain of the emitter follower stage. (Again you may need to add a 220 k Ω resistor to ground after C_{out} to keep the dc level at the scope input near ground.) You may want to put the

scope on ac coupling when you probe points with large dc offsets but switch it back to DC if you want to measure quiescent voltages.

Attach a $560\ \Omega$ load from the output to ground. What fraction of the unloaded output do you now see? Is this what you expect?

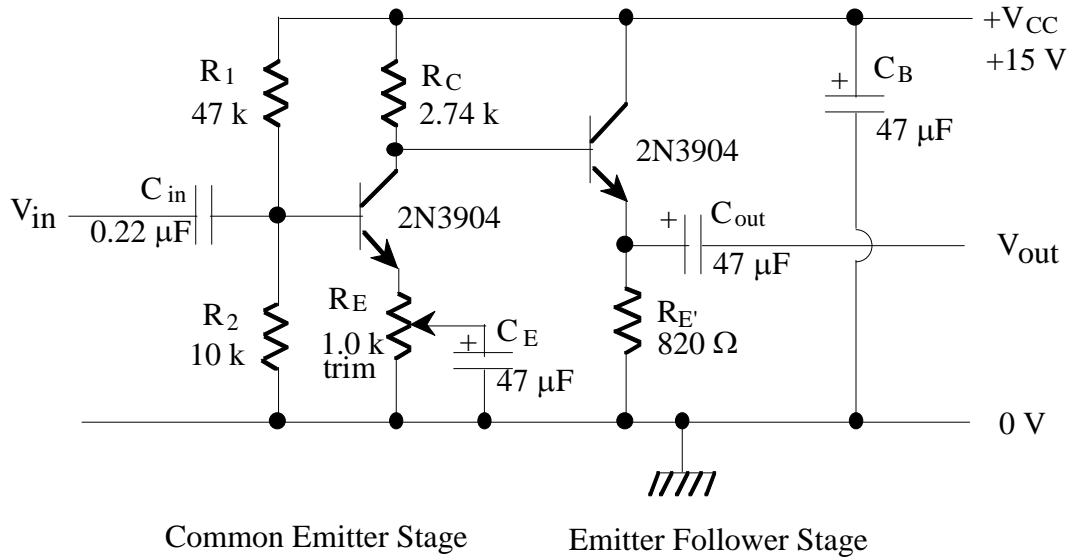


Figure 7.5 Complete Two-stage Amplifier Circuit

FINAL TESTS

Reset the gain to -25 with the $1\ \text{k}\Omega$ source resistor and the $560\ \Omega$ output load in place. Check the linearity of the amplifier for $10\ \text{kHz}$ sine waves by measuring the output amplitude at several input amplitudes, extending up into the clipped regime. Graph V_{out} versus V_{in} . The slope should equal the gain in the linear region of the graph.

Set the amplitude to be about one half the clipped value and then determine the upper and lower cut-off frequencies f_+ and f_- by varying the frequency of the sine waves. Extra credit: Can you understand the origin of these frequency cutoffs?